IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

SOLAS OLED LTD.,

Plaintiff,

v.

SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG DISPLAY CO., LTD., AND SAMSUNG ELECTRONICS CO., LTD.,

Defendants.

Civil Action No. 2:21-cv-00104-JRG

DEFENDANTS SAMSUNG DISPLAY CO., LTD., SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG ELECTRONICS AMERICA, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

The constructions proposed by Defendants Samsung Display Co., Ltd., Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (collectively "Defendants"), reflect the meaning of the technical terms at issue to a person of ordinary skill in the art (POSITA) at the time of the invention. These constructions are based on the claim language, the specifications, and the file histories. They are further supported by pertinent extrinsic evidence.

Solas's constructions, by contrast, are inconsistent not only with the intrinsic and extrinsic evidence, but also with constructions that Solas agreed to in its prior litigation on the same patents. For most terms at issue, Solas also relies on a declaration of its expert, the value of which is questionable: Mr. Flasck admitted he did not see and sign the original version served on Defendants (despite it bearing his signature), Ex. 3 (Flasck Dep.), 17:11–24; 14:9–12 (testifying he saw a different version). In fact, in deposition Mr. Flasck offered sworn testimony contradicting assertions of his declaration, making admissions that further support Defendants' constructions.

II. ARGUMENT

A. Background of the '042 Patent

The '042 patent generally relates to an active-matrix organic electroluminescent display (OLED) and a method for driving the display. *See, e.g.*, Ex. 1 ('042 patent), 2:32–34. At the time of the purported invention there were two fundamentally different types of OLED displays: 1) current-controlled displays, in which image data is provided as a current, and 2) voltage-controlled displays, in which image data is provided as a voltage.[1] The patent describes problems associated

[1] In both types of displays, the organic light emitting element generates light based on the amount of current passing through it, and thus the light emission element may itself be called a "current control type (or a current drive type) of light emission element." Ex. 2 ('615 patent), 1:19–26. This is different from whether the pixels of the display receive image data as a current or a voltage value, which defines whether the display is a current-controlled (*i.e.*, current-

with "conventional voltage-controlled" displays, in which "the luminance and tone are controlled by the signal *voltage*."[2] *Id.*, 2:11–14. In particular, the patent explains that it is "difficult to uniquely designate the current value" flowing through the OLED (and hence the light output) in voltage-controlled displays because relevant characteristics of transistors such as threshold voltage—*i.e.*, the voltage at which the transistor transitions from the OFF state to the ON state—may change due to ambient temperature or extended use. *Id.*, 2:7–11. These difficulties led to "variations in luminance on the display screen" of such displays and lower image quality. *Id.*, 2:23–24. According to the patent, its invention makes improvements to a different (current-controlled) type of display to avoid these difficulties. The patent describes a three-transistor current-controlled pixel circuit in which luminance and tone are controlled by a "designating current" rather than a signal voltage, and a method of driving that circuit. *Id.*, 2:32–45.

The asserted claims of the '042 patent stand rejected in ongoing *ex parte* reexamination ("EPR") proceedings. (*See* Dkt. 66.) In a recent office action, the Examiner found that under the broadest-reasonable-interpretation standard, certain claim elements should be construed as means-plus-function under 35 U.S.C. § 112(6)—although the Examiner's invalidity findings apply equally whether the claim elements are construed that way or not. The Examiner directed Solas to respond to these claim interpretations. Ex. 5 (2/2/2022 Office Action), 13:2–18. Because Solas has not yet done so, and because the Examiner will issue a next (and presumptively final) office action evaluating Solas's response, the intrinsic evidence will continue to evolve in the EPR proceedings. Defendants further note that the Examiner's interpretations (1) are consistent with Defendants' constructions and (2) highlight how Solas's positions contravene even the broadest-reasonable-

programmed) display or a voltage-controlled (*i.e.*, voltage programmed) display, as Solas's expert confirmed, *see* Ex. 3, 184:3–185:15.

[2] All emphasis has been added unless otherwise noted.

interpretation of the claim language. To the extent that developments in the ongoing prosecution warrant modifications to claim constructions, Defendants will apprise the Court.[3]

B. Disputed Terms of the '042 Patent[4]

1. "the selection period" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"the time interval during which the ON voltage is applied to one selection scan line"	"time period during which a plurality of pixel circuits is selected"

It is undisputed that the claim term "the selection period" does not have a plain and ordinary meaning. The patent, however, explains its meaning, and the parties even agree on the passage that most clearly does so: Column 9, lines 22–27, which defines that "***[a] period in which*** the selection scan driver 5 ***applies the ON voltage V_{ON} to the selection scan line X_i in the ith row and thereby selects the selection scan line X_i*** in the ith row ***is called a selection period T_{SE}*** of the ith row." *See* Op. Br., 5. As this passage states, the "selection period" is the time interval during which a single selection scan line is selected by applying an ON voltage—which is Defendants' proposal.

The remainder of the specification likewise supports Defendants' construction. The specification explains that one selection scan line is selected at a time, where "selecting" a scan line means applying an ON voltage to it: "while applying the ON voltage V_{ON} to the selection scan line X_i, the selection scan driver 5 applies the OFF voltage V_{OFF} to the other selection scan lines X_1 to X_m (except for the selection scan line X_i)" such that "the selection periods T_{SE} of the selection scan lines X_1 to X_m do not overlap each other." Ex. 1, 9:27–32. The specification consistently and

[3] Defendants moved to stay this case pending the EPR (Dkt. 45), and believe the EPR proceedings squarely raising issues of claim interpretation, and creating relevant new intrinsic evidence, further support stay of this case. Defendants have also moved for a continuance of *Markman* proceedings in view of the first office action of the EPR. (Dkt. 67).

[4] A POSITA of the '042 and '615 patents would have a degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active matrix display design and/or manufacturing, or could substitute additional relevant education for experience.

uniformly describes the selection period in this manner. *See, e.g.*, *id.*, 4:33–34, 9:3–57, 12:35–52, 21:46–49, 25:3–6, 26:65–27:1; Fig. 4. Even apart from the definition of Column 9, this consistent usage defines "the selection period" by implication. *See Irdeto Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004) ("Even when guidance is not provided in explicit definitional format, the specification may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents."); *see Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc); *Trs. of Columbia Univ. in City of N.Y. v. Symantec Corp.*, 811 F.3d 1359, 1364 (Fed. Cir. 2016); *Nystrom v. TREX Co.*, 424 F.3d 1136, 1144–45 (Fed. Cir. 2005).

Solas advances two main criticisms of Defendants' construction, neither of which has merit. First, Solas argues that "selection" does not mean applying an ON voltage. This is flatly inconsistent with the specification. Solas itself quotes Column 9, lines 22–27 to explain "the selection period," yet resorts to using ellipses to omit the clear statement that a selection period is "[a] period in which the selection scan driver 5 ***applies the ON voltage V_{ON} to the selection scan line X_i.***" Op. Br., 5. As Solas's brief recognizes, this passage is not simply describing a preferred embodiment. And Solas cannot credibly claim that Defendants' construction limits the term to a preferred embodiment, which it does not do. Solas adds a strawman argument that Defendants' construction limits the ON voltage to a specific voltage value or type of transistor (NMOS), when the construction does no such thing. The construction does not require any particular voltage value or transistor; even Solas's expert admitted that *both* types of transistors (PMOS and NMOS) have an ON voltage, *i.e.*, a voltage that turns the transistor on. Ex. 3, 105:2–7.

Second, Solas argues that the "selection period" does not refer to selection of one scan line (*i.e.*, an ith row scan line), but rather a plurality of scan lines. Op. Br., 6. That is incorrect. The

specification defines a selection period as the selection of a single scan line, "scan line X_i in the ith row": "***[a] period*** in which the selection scan driver 5 ***applies the ON voltage V_{ON} to the selection scan line X_i in the ith row*** and thereby selects the selection scan line X_i in the ith row ***is called a selection period T_{SE}*** of the ith row." Ex. 1, 9:22–27. Solas itself acknowledges "the 'selection period' is something that belongs to a row of pixel circuits," Op. Br., 5, and the patent is clear that each row of pixel circuits is connected to a single selection scan line. *See, e.g.*, Ex. 1, 5:15–18 ("The n pixels $P_{i,1}$ to $P_{i,n}$ arranged along the row direction are connected to the selection scan line X_i and voltage supply line Z_i in the ith row."). And Solas fails to identify any embodiment that selects a plurality of scan lines. None does. *See, e.g.*, *id*., 21:46–49, 25:1–6, 26:65–27:1; Figs. 1, 10–12. Solas's concession that the selection period corresponds to selection of a single row of pixel circuits acknowledges that a single scan line is selected, as Defendants propose.

Solas's criticism of Defendants' construction is based on Solas's faulty premise that the claim should be interpreted to require selecting a "***plurality*** of selection scan lines" in a selection period. Solas's argument is belied by the definition of "selection period," which as discussed above refers explicitly to selecting a single scan line, *i.e.*, "the selection scan line X_i in the ith row." Further, the specification contains no disclosure of selecting more than one selection scan line in a selection period. Tellingly, Solas identifies none. To the contrary, *every* disclosed embodiment describes a selection scan driver that sequentially selects each (singular) selection scan line, one at a time. *Id.*, 9:3–32 ("the selection scan driver 5 sequentially selects the selection scan lines X_1 to X_m by sequentially outputting selection signals in order from the selection scan line X_1 to the selection scan line X_m (the selection scan line X_m is followed by the selection scan line X_1)"); *see id*., 4:33–34, 21:46–49, 25:3–6, 26:65–27:1; Ex. 3, 126:7–127:2 (admitting Figure 4 shows one selection scan line is selected in each selection period). Indeed, in the EPR, the Examiner has found

that, even under the broadest-reasonable-interpretation standard, "the selection period" refers to selecting one selection scan line at a time. Ex. 5, 12:20–27.[5]

While Solas argues that the claim refers to selecting multiple selection lines at a time, Op. Br., 6, such a reading is inconsistent with the patent's disclosures. There is no embodiment in which multiple selection scan lines are selected in one selection period. And, because selection of a ***single*** scan line would not fall with the scope of a construction requiring at a minimum that two or more (*i.e.*, a ***plurality***) be selected, Solas's reading of the claim would *exclude* every disclosed embodiment. "[A] claim construction that excludes the preferred embodiment is rarely, if ever, correct." *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1378–79 (Fed. Cir. 2013).

Finally, Solas contends that because "multiple things occur[]" in the selection period, it is improper to define it based on "selecting the selection scan lines," *i.e.*, "when—and only when—the ON voltage is applied." Op. Br., 6. Solas's criticism rests on a non-sequitur. The specification defines the selection *period* as the time interval during which one selection scan line is selected. The claims recite certain things that must occur during that period. But it is the selection of a selection scan line through the application of an ON voltage that marks the beginning and end of the selection period. Indeed, the specification explains that the selection scan driver "keeps applying the ON voltage" during the different parts of the selection period. Ex. 1, 13:55–58.

Solas's expert agrees the selection period should be defined as having a "specific beginning (*e.g.*, T1) and a specific end (*e.g.*, T2)." Op. Br., Ex. 7 (Flasck Dec.), ¶ 42. Defendants' construction does so, while Solas's does not. As Defendants' construction conveys, the selection

[5] In prosecuting a European counterpart, the applicants distinguished prior art on the basis that the claimed invention carries out a reset and writing process in the same selection period. Ex. 6, 4–5. The applicants notably defined each selection period by a "pulse" formed by applying an ON voltage to a selection scan line. *Id.* ("The scanning line driving circuit makes two selections (two pulses) of a first scan signal SC1 and a second scan signal SC2 for each scanning line").

period begins when the ON voltage is applied to a selection scan line, and ends when the ON voltage ceases to be applied. Solas's construction ("time period during which a plurality of pixel circuits is selected") fails to indicate what begins and ends the selection period, leaving the time interval unbounded and entirely unclear. Solas's construction also yields absurd results. As Figure 4 shows, *at every point in time* during operation of the patent's display, one selection scan line connected to a row of pixel circuits—*i.e.*, to a plurality of pixel circuits—is selected. Thus, under Solas's theory, a plurality of pixel circuits will be selected *at all times*, meaning that *every* time interval shown in Figure 4 would be a "selection period." But Figure 4 shows, and the specification explains, that it contains *non-selection* periods. To the extent Solas's proposal could—contrary to its language—be read to allow for non-selection periods, it would be entirely indeterminate; there would be no principled way to identify the beginning and end of the period, and any number of different intervals could equally be called "selection periods." Solas's proposal is thus not only vague and unhelpful, but read literally it contravenes the clear disclosures of the patent.

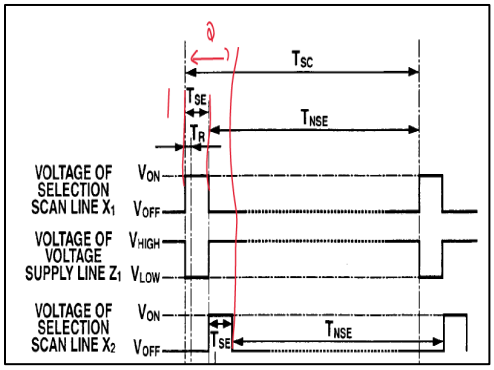
2. "sequentially selects said plurality of selection scan lines in each selection period" (claim 1)

Defendants' Proposal	**Plaintiff's Proposal**
"applies an ON voltage to the selection scan lines one after the other, such that one selection scan line is selected in each selection period"	Plain and ordinary meaning

Defendants' construction accords the term "sequentially selects said plurality of selection scan lines in each selection period" its clear meaning in the patent, "applies an ON voltage to the selection scan lines one after the other, such that one selection scan line is selected in each selection period." This flows from the intrinsic record's disclosures that each selection scan line is selected one after the other. *See, e.g.*, Ex. 1, 9:3–33. In the EPR, the Examiner has found that even under the broadest-reasonable-interpretation standard, this term refers to selecting one selection scan line at a time, in sequence. Ex. 5, 12:20–27. The dictionaries Solas cites also show Defendants'

construction is consistent with the standard meaning of "sequential," *i.e.*, following one after the other. *See* Op. Br., 7 (citing dictionaries defining "sequential" and "sequence" as "following in sequence" and "following of one thing after another"). In contrast, Solas's proposal fails to clarify the term's meaning.

As Solas's expert confirmed in deposition, the patent teaches that each selection scan line is selected one after the other, in sequence. For instance, asked to identify one selection period using the annotated timing diagram of Figure 4 shown here, he identified the time interval during which the voltage of one selection scan line is "ON" (labeled in red as "1").



Ex. 3, 126:14–127:2 ("[O]n the first line when the – when the voltage goes high, there is one plurality of pixel circuits that are selected, that is, the pixel circuits of the first row."); *see id.*, 124:14–127:2; Ex. 7 (Flasck Dep. Ex. 9), 2. He further confirmed that a first selection scan line being applied with the ON voltage and then a second selection scan line being applied with the ON voltage (labeled in red as "2") constitutes ***two*** selection periods, not one. *Id.* ("[I]n, applying . . . Solas's proposed construction, that would be two selection time periods.").

Solas posits "scenarios where the selection of scan lines may overlap or may occur during the same selection period." Op. Br., 7. Insofar as Solas interprets this claim term to mean selecting *a plurality* of scan lines at the same time or in the same selection period, there is no support in the patent for Solas's interpretation. On the contrary, the patent uniformly describes selecting a single selection scan line in each selection period, and Solas's interpretation would exclude all the patent's embodiments. "A claim construction that excludes the preferred embodiment is rarely, if ever, correct." *SynQor*, 709 F.3d at 1378–79. And the specification "is the single best guide" to

the meaning of a term. *See Phillips*, 415 F.3d at 1315 (citation omitted). As Solas's construction would exclude all of the disclosed embodiments and contravene the teachings of the specification, it should be rejected.

3. "pixel circuit" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"the circuit that includes the switching and storage elements used to drive a light emission element of a pixel"	Plain and ordinary meaning, i.e., the circuit that includes switching and/or storage elements used to drive a light emission element of a pixel

The parties' dispute over the term "pixel circuit" centers on how it can be determined which switching and storage elements comprise the pixel circuit. Defendants' proposal provides a clear answer based on the claim language, the specification, and the term's general usage in the art: "the circuit that includes the switching and storage elements used to drive a light emission element of a pixel." Solas's expert admits that Defendants' construction is consistent with the understanding of a POSITA. Ex. 3, 164:17–166:15 ("[A] POSITA would understand that a pixel circuit are the – are the switches and the storage elements in the pixel that are used to drive the light emission element of a pixel . . . It would include the drive transistor, the capacitor, the holding transistor, the selection transistor [and] the wiring connecting them all"). Solas, in contrast, proposes vague language providing no basis to identify which "switching and/or storage elements" are included in the circuit and which are not, leaving the meaning of "pixel circuit" indeterminate. Solas's construction would lead to the absurd result that various different transistors or sets of transistors (*i.e.*, switching elements), or capacitors (*i.e.*, storage elements), or combinations of them in the same device could be called the "pixel circuit."

The patent explains that each "pixel $P_{i,j}$ includes … a pixel circuit $D_{i,j}$ which is formed around the organic electroluminescent element $E_{i,j}$, and drives it." Ex. 1, 5:31–37. Consistent with Defendants' construction, the patent explains that the set of transistors and capacitors that drive

the light-emitting element are called the pixel circuit. As shown, *e.g.*, in Figure 1, the pixel circuit includes three switching elements (transistors 21, 22, and 23) and one storage element (capacitor 24). The specification describes the operation of each element in driving the light emission element E. *See, e.g.*, *id.*, 19:50–21:23. In the EPR, the Examiner found that even under the broadest-reasonable-interpretation, the pixel circuit includes each of these elements. Ex. 5, 10:10–12.

Solas purports to take issue with Defendants' proposal because "it refers to 'the switching and storage elements,'" yet Solas's construction also references both switching and storage elements. Solas then suggests, inconsistently, that Defendants' construction is either superfluous in light of the claim language, or too expansive. Neither criticism has merit. Defendants' construction is not superfluous, as it clarifies *which* switching and storage elements comprise the pixel circuit. And Solas's assertion that it is too expansive rests on a mischaracterization that Defendants' construction may encompass additional elements such as the switches S of the third embodiment Solas identifies. Defendants' proposal does not. Rather, those switches are part of a separately claimed element, the data driving circuit, as Solas admits. Op. Br., 9. In fact, it is Solas's ambiguous, open-ended construction that would allow for picking and choosing elements, the very flaw that Solas misattributes to Defendants' proposal.

4. "current lines" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"conductive lines each of which connects a data driving circuit to a plurality of pixel circuits and carries both a designating current and a reset voltage"	Plain and ordinary meaning, i.e., lines through which a current flows

The parties have two main disputes over "current lines." First, Solas itself argued in its prior suit over this same patent that the plain and ordinary meaning of "current lines" in the '042 patent is "***conductive*** lines for carrying current," Ex. 8 at 5, but Solas now criticizes Defendants' proposal for stating the current lines are "conductive." To the extent Solas is arguing that

"conductive" is unnecessary as superfluous, Defendants disagree. Defendants believe that stating that these lines are conductive is critical to assisting the factfinder in understanding the claims.

The intrinsic evidence and plain meaning have not changed since Solas agreed that the claimed current lines are "conductive lines." All that changed is that Defendants pointed out in a proceeding on different patents that transistors are not conductive lines. Solas's expert admits that Solas now removes the word "conductive" in an attempt to read "current lines" on other circuit elements, *e.g.,* transistors, in the pixel circuit—wholly inconsistent with the patent and what Solas admitted is the plain meaning. Ex. 4, ¶ 56 ("The reason for this change is simple. I understand that Samsung has argued, in a different context involving different patents, that a line which contains a semiconductor portion which is switched by a transistor gate to create a conductive channel between a transistor's source and drain is not a 'conductive line[.]'"); Ex. 3, 155:8–15.

Solas's new position and construction are inconsistent not only with the term's plain meaning, but with the intrinsic record. The patent consistently identifies transistors and current lines as separate elements. *E.g.*, Ex. 1, 7:65–8:9; cl. 6, Fig. 1. And, Solas is plainly incorrect in suggesting that the fact that charge can flow through something at a point in time means it is "conductive." Ex. 4, ¶ 56. For example, lightning flows through air, but that does not make air a "conductive" material. Likewise, current may flow through a transistor if an adequate electric field is applied, but that does not make the pathway through a transistor a conductive line.

The second dispute concerns the portion of Defendants' construction that a "current line" connects a data driving circuit to a plurality of pixel circuits and carries both a designating current and a reset voltage. Solas does not contend this is incorrect, just that it is unnecessary to articulate because these features of current lines are specified in other language of the claim. Op. Br., 10. Contrary to Solas's argument, the fact that Defendants' construction aligns with and is supported

by the remaining claim language is strong evidence in its favor. *Phillips*, 415 F.3d at 1314 ("the claims themselves provide substantial guidance as to the meaning" of terms). Moreover, while Solas acknowledges that the claim language contains these requirements for "current lines," Solas also asserts that this aspect of Defendants' construction is somehow "not supported by the specification." Op. Br., 11. It is unclear what Solas means, but the fact that Solas simultaneously (1) acknowledges that the claim language requires that each current line connects a data driving circuit to a plurality of pixel circuits and carries both a designating current and a reset voltage requirements are required by the claim, but (2) argues (incorrectly) these requirements are not supported by the specification, underscores the need to include them in the construction.

Further, Solas's expert admits that the claim requires that each current line is connected to a data driving circuit and a plurality of pixel circuits. Ex. 3, 158:9–23. Consistent with the claim, every embodiment of the specification discloses that each current line is connected to a plurality of pixel circuits. Ex. 1, 5:18–20; *id.*, 21:46–49, 25:1–6, 26:65–27:1; Figs. 1, 10–12.

Solas appears to be attempting to interpret a "current line" to be part of the pixel circuit. *See* Dkt. 9 at 12 (Amended Complaint circling pixel circuit in red and highlighting alleged current line in pink). This cannot be correct, as the claim language and specification identify "current lines" and "pixel circuits" as separate structures. The claim states the current lines are "connected to," not part of, the pixel circuits. *See, e.g.*, *Becton Dickinson and Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) ("Where a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s].'"). As in *Becton Dickinson*, nothing in the claim suggests the pixel circuit and current line can be the same structure, and the specification confirms they are distinct elements. *Id.*; *see, e.g.*, Ex. 1, Fig. 1.

Finally, Solas attempts to sidestep a key difference between the parties' constructions: whether each current line must carry both a reset voltage and a designating current. Solas attempts to hide in the plural in suggesting that the claim already "require[s] that a 'designating current' and a 'reset voltage' be applied to a '***plurality*** of current ***lines***'" without addressing whether *each* current line must carry *both* of these signals. Op. Br., 10. However, Solas does not and cannot dispute that according to the patent, ***each*** current line carries both signals; this is central to the patent's alleged invention. Solas's expert admitted that his understanding of the claim accords with Defendants' proposal, *i.e.,* that the claim requires that each current line must carry both signals. *See, e.g.*, Ex. 3, 51:7–13 ("Q. And the current lines are what we talked about earlier, each of which is going to have that recent [*sic*] voltage followed by the designating current, right? A. That's how . . . the embodiments work. And I believe that's what's outlined in . . . claim 1 later on."); *see id.*, 160:24–161:25. The specification strongly supports this. In every embodiment, each current line carries both a reset voltage and a designating current. For example, annotated Figure 1 shows that each pixel circuit is connected to a current line Y, which is connected to a switch S (yellow) in the data driving circuit. The specification explains that the switch S "switches the state in which the current source driver 3 supplies the tone designating current I_{DATA} to the current line Y_j, and the state in which the reset voltage V_R is applied to the current line Y_j." Ex. 1, 12:16–21. Solas fails to identify any embodiment that would support a contrary reading.

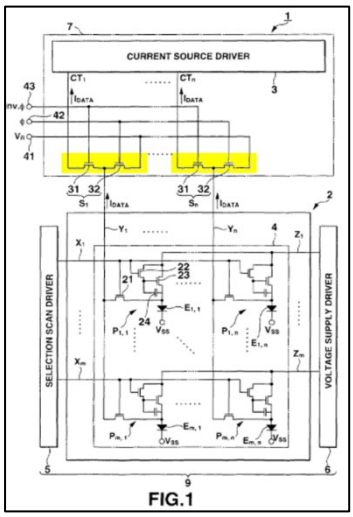


FIG.1

5. "designating current" (claim 1)

Defendants' Proposal	Plaintiff's Proposal
"current set to a constant value to control the luminance of the OLED"	Plain and ordinary meaning, i.e., current designating a value corresponding to an image signal

The term "designating current" has no customary meaning in the art, but rather is specific to the patent. Solas does not show otherwise. Defendants' proposal provides the term its meaning in the patent, "current set to a constant value to control the luminance of the OLED." Solas's proposal, in contrast, disregards the intrinsic evidence and leaves the meaning unclear.

Solas mainly attacks strawmen to dispute Defendants' proposal. Solas first argues that "the specification never describes the designating current as set to a constant value *during the first reset portion*." Op. Br., 12. Crucially, Solas fails to mention that there is no designating current applied during the first reset portion. Rather, a reset voltage, not a designating current, is applied in the reset portion. Solas's expert admitted as much in deposition. Ex. 3, 143:10–144:11. Thus, Solas's argument about the first reset portion is inapposite, if not nonsensical. Solas next suggests that there is claim language describing the designating current changing, but that is also incorrect. Solas's expert admitted that the only purported "change" is that, during the first part of the selection period a designating current is not provided, while during a second part of the selection period a designating current is provided. *Id*., 144:19–145:2. This is fully consistent with Defendants' proposal: the current is set to a constant value when it is applied. The claim language, like the specification, does not describe any change in the designating current during the part of the selection period in which a designating current is applied.

As to the second portion of the selection period, when the designating current is actually applied, Solas admits that "the specification provides that the designating current in one embodiment is held constant." Op. Br., 12. Solas's only basis for suggesting that a designating current is not held constant in any disclosure is its incorrect assertion that Figure 9 purportedly shows the designating current is not held constant in this period but rather "asymptotically approaches a stable value." *Id.* Solas ignores that the specification explicitly states that Figure 9

shows the designating current "is held constant" in the second portion of the selection period. Ex. 1, 17:63–18:18 ("***Until the end of the selection period T_{SE}*** of the ith row…the current value of **the *tone designating current I_{DATA} . . . is held constant in accordance with the image signal***.").

Figure 9 thus cannot mean, as Solas suggests, that the designating current is not held constant in this period. In any event, Defendants' proposal states that the designating current is "set to" a constant value, and even Solas's flawed argument about Figure 9 does not contest this. Figure 9 shows that the data driving circuit sets the designating current to a specific (constant) current value, and that—in the real world—this current value takes time to reach a steady state when provided to the current line. *See, e.g.*, Ex. 1, 17:63–18:18; *cf.* 14:8–10 ("In this state, as shown in Fig. 4, the voltage of the current line Y_j drops until the tone designating current I_{DATA} becomes steady."); 13:28–30 ("the tone designating current I_{DATA} having a steady current value can be rapidly written in the next selection period T_{SE}"); Ex. 3, 151:3–19. The patent describes "equivalent" functionality for all embodiments. *See, e.g.*, Ex. 1, 23:33–46, 22:8–16, 26:18–21, 25:61–66, 27:46–49, 27:13–19.

As the intrinsic evidence establishes, it is fundamental to the patent that the designating current is set to a constant value during the second part of the selection period. This is because, as the patent explains, the designating current is "a desired current value" that allows the light-emitting (EL) element to "emit light at a desired tone luminance." Ex. 1, 20:16–24. Indeed, "***the luminance . . . of the organic EL elements***" in the displays "***is uniquely determined by the current value of the tone designating current I_{DATA}*** which flows through the pixel circuits… in the selection period T_{SE}." *Id.*, 15:53–57. If this designating current value were allowed to vary during this part of the selection period, then the current value provided to the pixel would vary, and would not be the "desired current value." This would frustrate the very purpose of the patent, which is to

ensure that the specific value intended for each pixel is correctly provided by a constant current. *See, e.g.*, *id.*, 20:52–65.

At bottom, Solas misreads the claim language and specification in an apparent attempt to broaden the claims to cover voltage-controlled displays, when they are directed to current-controlled (*i.e.*, current-written) displays, as Solas's expert admits. Ex. 3, 42:15–43:7 ("[Claim 1] says that the current lines…supplies a designating current, using a current value corresponding to an image signal. So that, to me, says that it's a – it's a current-written device."). As Solas's expert confirmed, the limitation that the data driving circuit supplies a "designating current having a current value corresponding to an image signal" connotes a current-controlled display. *Id*. As he further confirmed, the key difference between voltage-controlled and current-controlled displays is that in a voltage-controlled display the image data is provided as a voltage, whereas in a current-controlled display the image data is provided as a current. *Id*. The claimed inventions being current-controlled is at the heart of the patent, which explicitly describes the alternative approach of voltage-controlled displays as unsuitable. Ex. 1, 2:7–28. Solas's efforts to read the claims on voltage-controlled displays should be rejected.

C. Background of the '615 Patent

The '615 patent is generally directed to a light emission drive circuit used to drive the individual pixels of an OLED display. Ex. 2 ('615 patent), 48:23–49:5. As with the '042 patent, the '615 patent describes problems associated with voltage-controlled systems because the current value supplied to the OLED "is controlled by controlling the voltage value of the voltage . . . to be applied to each display pixel." *Id.*, 3:21–62. The '615 patent describes a "light emission drive circuit" that controls the luminance of the OLED via a gradation sequence current, *see, e.g.*, *id.*, 18:3–30, and a driving approach for this circuit in which first a precharge voltage is provided to the light emission drive circuit through the data line, after which the gradation sequence current is

provided to the light emission drive circuit via the data line, *id*.

D. Disputed Terms of the '615 Patent

1. "exceeding a threshold value" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"greater than a threshold value"	Plain and ordinary meaning, i.e., has an absolute value larger than that of a threshold value.

The sole dispute over this term concerns the meaning of "exceeding." "[E]xceeding" has a commonly understood and accepted meaning—*i.e.*, to be greater than. *See, e.g.*, Ex. 9 (Microsoft Encarta College Dictionary) at 497 (defining "exceed" as "**BE GREATER THAN** to be greater than something in quantity, degree, or scope") (emphasis in original); Ex. 10 (Webster's unabridged dictionary) (defining "exceed" as "to be greater, as in quantity or degree"). Defendants' construction gives the claim term its plain and ordinary meaning. Solas cannot contest this, nor does Solas argue that the patentee acted as its own lexicographer or disclaimed the plain and ordinary meaning. Solas nonetheless urges the Court to depart from the plain meaning and rewrite the claim, to replace "exceeding" with a different concept—"greater than" some values and "less than" others—by grafting on the concept of absolute values. Solas's construction is inconsistent with the claim language and the other intrinsic evidence, and should be rejected.

Claim 11 states "the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line." Ex. 2, 48:56–58. Claim 11 uses the term "exceeding" according to its plain meaning, *i.e.*, greater than. So, too, does the remainder of the patent. *See, e.g.*, *id.*, 23:41–44 ("In particularly [*sic*], in the lowest luminance voltage Vlsb, the ratio of the electric charges needed by the threshold voltage Vth13 in the all electric charges ***exceeds 50%***.").

Solas does not dispute that "exceeding" should be given its plain meaning, nor that Defendants' construction represents the term's standard meaning. Solas cannot credibly claim its

proposal, "has *an absolute value larger than that of*," represents the plain meaning. Tellingly, Solas cites no dictionary. Rather, Solas seeks to rewrite claim 11 to reach displays not only in which the precharge voltage is "greater than" than the threshold value (as claim 11 states), but also those in which the precharge voltage is "less than" or "more negative" than (*i.e.*, falls below) the threshold value. Op. Br., 14–15. But it is well known, including to POSITAs, that being "less than" a value is the antithesis of "exceeding" that value. Solas even acknowledges at one point that "if the threshold is positive, exceeding that voltage means being ***more positive***, and if the threshold is negative, exceeding that voltage means being ***more positive***." *Id.* (emphasis Solas's). That is, of course, correct, and consistent with Defendants' proposal, *not* Solas's.

Solas's proposal also disregards that the patentee used different language in other claims when the patentee intended to refer to absolute values. "[D]ifferent words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope." *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1369 (Fed. Cir. 2007). Claim 1, unlike claim 11, contains a limitation of "a voltage having *an absolute value that is larger than* an absolute value of a threshold voltage of the drive transistor," Ex. 2, 46:35–37. Claim 1 shows that when the patentee intended to refer to absolute values, it did so explicitly. As Solas itself argues elsewhere in its brief, "there is no basis for assigning the same construction to two different terms" since the inventors "intentionally chose the words and phrases for a reason." Op. Br., 24. Moreover, claim 1 draws a distinction between "a voltage *having an absolute value that is larger than* the absolute value of a threshold voltage" and "a voltage *exceeding* a minimum luminance voltage." Ex. 2, 46:35–38. Claim 1's different language further undercuts Solas's proposal.

Solas's argument that "there is nothing in the specification that suggests a different comparison" being made in claims 1 and 11, Op. Br., 15, is also incorrect. Even putting aside that

it is the claim language that governs, Solas ignores the specification's most relevant passage on this issue, which shows the patentee explicitly referred to absolute values when that concept was intended. In comparing the value of a precharge voltage (Vpre13) to the threshold voltage of a drive transistor (Vth13), the specification first states "*the absolute value of* the voltage Vpre13 is larger than *the absolute value of* a gate-to-source voltage Vth13 of the drive transistor Tr 13." Ex. 2, 19:5–7. The specification then states in the next sentence that "***[i]n an n channel transistor***, the voltage Vpre13 is ***higher than the threshold voltage*** Vth13." *Id*., 19:7–9. Thus, the patent is explicit that it refers to a comparison of absolute values (as in claim 1) when it intends to include both n-channel and p-channel transistors; but it refers to a precharge voltage "higher than" the threshold value (as in claim 11) when discussing n-channel transistors. Indeed, Solas's expert acknowledged the significance of the difference in language:

> Q. So if they wanted to talk about PMOS and NMOS, they would talk about absolute value; right? A. That's one way of doing it.
>
> Q. But if they wanted to talk about just NMOS, they would, for instance, say that the precharge voltage is higher than the threshold voltage?
>
> A. If they were only talking about NMOS, then they could simply say the VPRE is larger than the threshold voltage. The precharge -- ***if they were only talking about NMOS, they could simply say*** the pre- -- ***the precharge voltage is larger than the threshold voltage***.
>
> Q. And "larger," you mean a higher voltage?
>
> A. Yes.
>
> Q. And so if the patent had said that, would you then agree that the claim was directed at NMOS?
>
> A. ***If the patent had said*** the -- ***that the precharge voltage was higher than the threshold voltage, then I don't see how it would work with PMOS. So I would say that it effectively was limited to NMOS***.

Ex. 3, 182:3–183:2 (objections omitted).

Solas's criticism of Defendants' construction also rests on a faulty premise: that claim 11

must cover both n-channel and p-channel transistors. Op. Br., 13–16. The claim language and specification contradict such a notion. The patentee in claim 1, and the specification, explicitly refers to absolute values when intending to encompass both types of transistors, and uses different language ("larger than" or "exceeding") in claim 11 and the specification when addressing one type. That claim 11 is narrower in this respect than claim 1 is unsurprising, given the patent's focus on devices using n-channel transistors. Every embodiment uses n-channel transistors. *E.g.*, Ex. 2, Figs. 1, 3–4, 11–12, 14, 21. Solas notes a statement at the end of the specification that p-channel transistors can also be used. Op. Br., 13 (citing Ex. 2, 46:8–11). That does not help Solas. Claim 1—whose language is different—covers this. Claim 11 does not. It is well-established that some claims may cover some embodiments, and other claims other embodiments; not every claim must cover every embodiment. *PSN Illinois, LLC v. Ivoclar Vivadent, Inc.*, 525 F.3d 1159, 1166 (Fed. Cir. 2008) ("[A]ll claims [need not] cover all embodiments. Instead, courts must recognize that disclosed embodiments may be within the scope of other allowed but unasserted claims.").

Solas's construction would also lead to absurd results. For example, under Solas's construction, claim 11 would read on a display in which a precharge voltage of -2 is applied to a transistor having a threshold voltage of +1, because the *absolute value* of -2 is greater than the absolute value of +1. As Solas's expert admitted, this makes no sense: Presented with this exact hypothetical, he conceded, "[y]es, that would be a problem." Ex. 3, 183:16–20. Solas attempts to sidestep this fatal flaw by arguing that circuits using n-channel transistors will "generally" use positive voltages, while circuits using p-channel transistors will generally use negative voltages. Op. Br., 15. But that does not negate the fact that Solas's construction would lead to the nonsensical result that a precharge value of -2 would "exceed" a threshold value of +1.

Recognizing its proposal yields nonsensical results, Solas shifts course and states it "would

not object to construing 'exceeding a threshold value' to mean 'having a value more positive than the threshold value, if the threshold value is positive; or having a value more negative than the threshold value, if the threshold value is negative.'" *Id.*, 15–16. But "exceeding" does not mean "greater than, if positive; less than, if negative." Solas's fallback is flatly inconsistent with the plain meaning of "exceeding" and the intrinsic evidence, transparently seeking to rewrite the claim.

2. "precharge voltage" (claim 11)

As Solas acknowledges, the specification describes "*two different voltages* applied to *two different components*. The first voltage, Vpre, is the voltage applied to the data line DL . . . . The second voltage, Vpre13, is the voltage applied to the capacitor Cs and appears across the gate source of transistor T13 . . . ." Op. Br., 17 (emphasis in original). Solas states "a POSITA would easily be able to determine that the 'precharge voltage' in claim 11 corresponds to the 'precharge voltage Vpre,' and *not* Vpre13." *Id*., 18 (emphasis in original). While the claim language lacks clarity, in an effort to narrow the disputes, Defendants agree to no longer challenge definiteness of "precharge voltage" provided that it is interpreted to have the meaning Solas argues in its brief: the claimed "precharge voltage" refers to the precharge voltage Vpre applied to the data line, and not a voltage such as Vpre 13 applied to the capacitor.

3. "light emission control section" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"drive transistor"	Plain and ordinary meaning, i.e., circuit section that controls light emission.

Defendants' construction of the term "light emission control section" as "drive transistor" is the same construction *Solas agreed to* for this patent in *Solas OLED Ltd. v. HP Inc.*, Case No. 6:19-cv-00631-ADA (W.D. Tex.) (the "HP Case"). Ex. 8 at 6. Remarkably, Solas's brief fails to mention that Defendants' construction is what Solas and its expert agreed to as the proper construction in prior litigation on the same patent, based on the same intrinsic evidence. Solas

provides no explanation for its about-face. Solas's expert, who also submitted a declaration in the HP Case accepting this construction, admitted he would not accept a claim construction for purposes of his declaration that he did not agree with. Ex. 3, 28:7–10. For these reasons and others, Solas's criticisms of the construction lack credibility. Moreover, Solas's new proposal, which does little more than rearrange the language of the claims, fails to provide any clarity.

Claim 11 requires both (1) a "light emission control section for generating a light emission drive current having a predetermined current value," and (2) a data driver that "applies a precharge voltage exceeding a threshold value of ***the drive transistor*** to the data line." Ex. 2, 48:29–31, 48:57–58. As discussed in Section III.D.6, the only potential antecedent basis for "the drive transistor" is the "light emission control section." Construing the light emission control section as "drive transistor" supplies the antecedent, as Solas's previously agreed-to construction recognized.

In addition, Defendants' construction gives the claim term its clear meaning in the specification, which explicitly equates the "light emission control section" with a "drive transistor." In describing "a light emission drive circuit DC according to the invention," the patent states the light emission drive circuit is configured to have "***a drive transistor (light emission control means)***." Ex. 2, 17:7–27. Moreover, as Solas's expert admits, in every embodiment the "light emission control section" is a drive transistor. Ex. 3, 196:18–22. Thus, the patent defines "light emission control section" as "drive transistor" explicitly or, at a minimum, by implication. *Irdeto*, 383 F.3d at 1300; *see Phillips*, 415 F.3d at 1321; *see Trs. of Columbia Univ.*, 811 F.3d at 1364; *Nystrom*, 424 F.3d at 1144–45.

Solas's construction, in contrast, is nothing more than functional language without structure, which would offer no way to determine the required structure. Were Solas's reading correct, the claim language would be subject to 35 U.S.C. § 112 ¶ 6, and the structure would be

the corresponding structure of the specification. As discussed above, the structure identified in the specification is the "the drive transistor," consistent with Defendants' construction.

Solas asserts that a POSITA would not understand the "light emission control section" to be a "drive transistor" because "claim 2 both requires a 'light emission control section' and specifies that the 'light emission control section ***includes*** a drive transistor." Op. Br., 19. This is incorrect (as Solas implicitly recognized in the HP Case), and ignores claim 2's full limitation:

> the light emission control section includes a drive transistor, in which a first end side of a current path through which the light emission drive current flows is connected to the light emission element and is connected to a first end side of the capacitance element, a supplying voltage for flowing the light emission drive current is applied to a second end side of the current path, and a control terminal for controlling a supplying state of the light emission drive current is connected to a second end side of the capacitance element

Ex. 2, 47:12–22. Claim 2 does not state a "light emission control section" *includes* additional circuit elements beyond a drive transistor; it merely indicates the light emission control section is ***connected*** to other circuit elements (*e.g.,* the light emission element and the capacitive element).

4. "writing control section" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"a selection transistor, which receives the gradation sequence signal and the precharge voltage from the data line"	Plain and ordinary meaning, i.e., circuit section that controls writing

The parties' dispute over "writing control section" is largely the same as that over the "light emission control section." Indeed, construing "writing control section" to mean "selection transistor" is consistent with Solas's position in the HP Case that "light emission control section" means "driving transistor." Similar to the "light emission control section" term, the specification defines the "writing control section" as a "selection transistor." Further, claim 11 expressly identifies the lines that carry signals "for controlling the operation state of writing control section" as the "***selection*** lines." Ex. 2, 48:41–43.

The patent expressly equates the "writing control section" with a "selection transistor": the patent states that "a light emission drive circuit DC according to the invention" is configured to have "***a selection transistor (writing control means)***." *Id.*, 17:7–27. Further, as Solas's expert admitted, in every embodiment the "writing control section" is a "selection transistor." Ex. 3, 79:23–80:11. The patent thus explicitly defines the "writing control section" as a "selection transistor," or, at the very least, does so "by implication." *Irdeto*, 383 F.3d at 1300; *see Phillips*, 415 F.3d at 1321; *Trs. of Columbia Univ.*, 811 F.3d at 1364; *Nystrom*, 424 F.3d at 1144–45.

Solas's construction does little more than rearrange the claim language, and is entirely functional, giving no indication of the structure. Were Solas's reading right, the claim would be subject to 35 U.S.C. § 112 ¶ 6, in which case the structure would be the corresponding structure of the specification. And, as discussed above, the structure identified in the specification is the "selection transistor," consistent with Defendants' construction. Indeed, Solas's expert admits that if the writing control section connotes any structure, "to a person of ordinary skill in the art . . . the use of a selection transistor would be the first thing that sprung to mind." Ex. 3, 87:22–88:7.

Finally, there is no merit to Solas argument that Defendants' construction is "flawed" because it purportedly "proposes to add an additional functional limitation: 'which receives the gradation sequence signal and the precharge voltage from the data line.'" Op. Br., 20–21. Solas ignores that what it terms an "additional functional limitation" is, in fact, an express requirement of the claim. Claim 11 explicitly states the "***writing control section*** . . . ***control[s] a supplying state of the electric charges based on the gradation sequence signal***"[6] and "the light emission drive circuit ***applies the precharge voltage*** applied to the data line to the electric charge

[6] Claim 11 further clarifies that the gradation sequence signal is supplied from the data lines. Ex. 2, 48:47–48 ("data lines to which the gradation sequence signals are supplied").

accumulating section ***via the writing control section***." Ex. 2, 48:56–61.

5. "voltage control section" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"holding transistor"	Plain and ordinary meaning, i.e., circuit section that controls voltage

The parties' dispute over "voltage control section" is largely the same as that over the terms, "light emission control section" and "writing control section." Construing "voltage control section" to mean "selection transistor" is again consistent with Solas's position in the HP Case that "light emission control section" means "driving transistor." Similarly, the specification defines the "voltage control section" as being a "holding transistor." Further, claim 11 expressly identifies the lines that carry signals "for controlling the operation state of the voltage control sections" as "***hold*** lines." Ex. 2, 48:44–46.

The patent expressly equates the "voltage control section" with a "holding transistor": the patent states that "a light emission drive circuit DC according to the invention" is configured to have "a holding transistor (voltage control means)." *Id.*, 17:7–27. Indeed, in every embodiment, the "voltage control section" is shown as a "holding transistor." The patent thus explicitly defines the "voltage control section" as a "holding transistor," or, at the very least, defines the term "by implication." *Irdeto*, 383 F.3d at 1300; *see Phillips*, 415 F.3d at 1321; *Trs. of Columbia Univ.*, 811 F.3d at 1364; *Nystrom*, 424 F.3d at 1144–45.

Solas's construction again does little more than rearrange the claim language, and is again entirely functional. If Solas's reading were right, it would suggest that the claim would be subject to 35 U.S.C. § 112 ¶ 6, in which case the structure would be limited to the corresponding structure of the specification and equivalents thereof. However, as discussed above, the structure identified in the specification is the "holding transistor" identified in Defendants' construction. Indeed, when asked in deposition if the "voltage control section connote[s] any specific structure to a person of

ordinary skill in the art," Solas's expert admitted that "the one that obviously comes to mind is a hold transistor as shown in the embodiments of the patent." Ex. 3, 85:14–21.

Finally, Solas erroneously asserts a POSITA would not understand the "voltage control section" to be a "holding transistor" under a premise that claim 2 "requires that 'the voltage control section ***includes*** a hold transistor." Op. Br., 21–22. That is incorrect and ignores the full limitation of claim 2 that "the voltage control section includes a hold transistor, in which one end side of a current path is connected to the second end side of the capacitance element, and a control terminal is connected to one of the hold lines." Ex. 2, 47:29–32. Claim 2 does not state that a "voltage control section" *includes* circuit elements beyond a holding transistor; to the contrary, the claim merely indicates the voltage control section is ***connected*** to other circuit elements (*e.g.*, the capacitive element).

6. "the drive transistor" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
Indefinite; alternatively no construction necessary if "light emission control section" is construed as "drive transistor."	Plain and ordinary meaning, not indefinite. Alternatively, "a drive transistor included in the light emission control section."

There is no prior recitation of a "drive transistor" in claim 11 to which the term "*the* drive transistor" could be referring. Therefore, it lacks antecedent basis and is presumptively indefinite unless a POSITA "would be able to ascertain the missing antecedent" despite "the undisputed defect in the claim." *Synqor, Inc. v. Artesyn Techs., Inc.*, No. 2:07-CV-497-TJW-CE, 2010 WL 2991037, at *27 (E.D. Tex. July 26, 2010). The only way a POSITA could ascertain the missing antecedent would be to interpret "light emission control section" as "drive transistor." This is consistent with the specification's clear and uniform disclosure that the "light emission control section" is the "drive transistor." *See, e.g.*, Ex. 2, 17:23, 25:46-53; *see also* Ex. 3, 196:18–22. *Solas itself agreed* in the HP Case that "light emission control section" should be construed as "drive

transistor." Ex. 8 at 6.

Solas remarkably fails to mention that it agreed to this construction in prior litigation, and provides no valid basis to deviate from it. The relevant evidence certainly has not changed. Solas even admits that the light emission control section must include a "drive transistor" to avoid indefiniteness. Op. Br., 22–23. The Court should adopt what Solas itself agreed in prior litigation is the proper construction of "light emission control section," *i.e.*, "drive transistor."

7. "light emission drive circuit" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"the circuit that includes the switching and storage elements used to drive a light emission element of a pixel"	Plain and ordinary meaning, i.e., circuit that controls light emission. Alternatively, "a drive circuit with a plurality of switching elements used to drive a light emission element of a pixel."

Similar to the "pixel circuit" term in the '042 patent, the parties' dispute as to the "light emission drive circuit" centers on how one can determine which elements are in the light emission drive circuit. Defendants' proposal provides a clear answer based on the claim language and the specification: "the circuit that includes the switching and storage elements used to drive a light emission element of a pixel." While Solas tries to fault Defendants' construction for corresponding to the construction of "pixel circuit" in the '042 patent, Solas's expert could not identify any differences in the structures of the "pixel circuit" of the '042 patent and "light emission drive circuit" of the '615 patent. Ex. 3, 168:8–169:17. In contrast, Solas proposes vague language that would leave the meaning of "light emission drive circuit" indeterminate. Solas's construction provides no basis to identify which "switching elements" are included in the circuit and which are not, and would lead to the absurd result that different individual transistors (*i.e.*, switching elements) and groups of transistors could variously be called the "light emission drive circuit."

The '615 patent discloses that the "light emission drive circuit DC according to the

invention" includes a number of transistors (switching elements) and a capacitor (storage element). Ex. 2, 17:7–43. As shown in the specification, for example in Figure 1, the light emission drive circuit includes three switching elements (transistors Tr11, Tr12, and Tr13) and one storage element (capacitor Cs). Defendants' construction is fully consistent with these disclosures.

Solas cites a passage of the specification that it suggests supports reading "light emission drive circuit" not to include "storage elements." Op. Br., 26. Solas disregards, however, that this passage is describing prior art, not the claimed invention. Ex. 2, 1:60–2:3. More to the point, claim 11 expressly requires that the light emission drive circuit contain an "electric charge accumulation section," *i.e.*, a storage element. Solas does not dispute this. When the specification describes "a light emission drive circuit DC according to the present invention" it even mentions "a capacitor (electric charge accumulating means and a capacity element)." Ex. 2, 17:28–29; *see* Ex. 3, 169:9–12. Thus, Solas's criticism of Defendants' construction is unfounded.

8. "data lines" (claim 11)

Defendants' Proposal	Plaintiff's Proposal
"conductive lines each of which connects a data driver to a plurality of light emission drive circuits and carries both a gradation sequence signal and a precharge voltage"	Plain and ordinary meaning, i.e., lines through which data is supplied. Alternatively, "lines to which the data driver supplies gradation sequence signals and applies a precharge voltage."

The intrinsic evidence establishes that "data lines" in the '615 patent mean "conductive lines each of which connects a data driver to a plurality of light emission drive circuits and carries both a gradation sequence signal and a precharge voltage," as Defendants propose. First, that the data lines are "conductive" follows from the plain meaning of the term. Solas admits "[t]he term 'data line' is readily understood by a POSITA, has a plain and ordinary meaning, and is used in the patent in accordance with that plain meaning, *i.e.*, ***conductive lines*** for supplying information." Op. Br., 26. Solas relies on the McGraw-Hill Dictionary defining "data transmission line" as "a

system of electrical ***conductors***." *Id*., 26–27. And, in the HP Case, Solas admitted "data lines" refers to "***conductive lines*** for supplying information." Ex. 8 at 7. While Solas admits the term "data lines" refers to "conductive" lines, Solas omits that important modifier and advances a proposal that does not require conductive lines. Solas's construction is thus erroneous.

Second, Defendants' construction makes clear, consistent with the intrinsic evidence, that each data line "connects a data driver to a plurality of light emission drive circuits and carries both a gradation sequence signal and a precharge voltage." Solas's brief does not contest that each data line carries both a gradation sequence signal and a precharge voltage. Nor could it, as these features of data lines are explicit in the claim language. Ex. 2, 48:47–61. Solas's expert admits that the claim means that all data lines must carry *both* types of signals. Ex. 3, 73:14–20 ("One of the limitations is a data driver which supplies the gradation sequence signals to the data lines. My interpretation of that is that ***the data lines all should receive*** the—***the gradation sequence signals and the precharge voltage*** at some point in time."); *see also id.*, 71:9–20.

Moreover, the specification explains that the display unit has "a data or signal driver 140 that is connected to the data line DL of the display panel 110 for supplying the precharge voltage Vpre to the display pixel EM ***via each data line DL*** in the precharge operation Tpre and supplying the gradation sequence signal . . . in accordance with the display data to the display pixel EM ***via each data DL*** in the writing operation time period Twr." Ex. 2, 35:2–10. For example, annotated Figure 1 shows the data line "DL" connected to the signal drive circuit "SDR" (yellow). The SDR contains a switch "SM" that allows the circuit to switch between supplying the precharge voltage "Vpre" on each data line during the

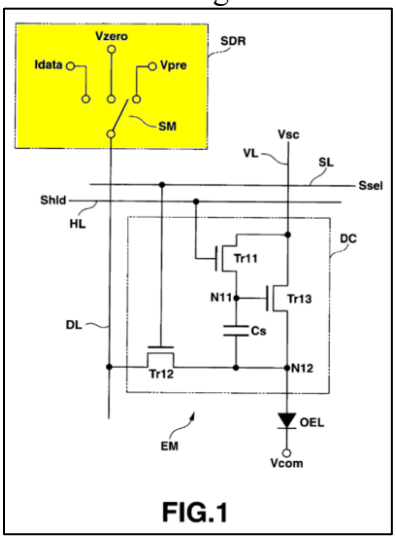


FIG.1

precharge time period and the gradation sequence current "Idata" on each data line during the writing operation time period. *See, e.g.*, *id.*, 18:21–29, 33:60–34:3. In every embodiment, each data line carries both types of signals. Solas does not identify any other designs, nor could it. This design is crucial to the circuit of the '615 patent.

Although the requirement that each data line carries both a gradation sequence signal and a precharge voltage is clear from the claim language and specification, Solas's constructions inexplicably omit it. Solas's alternative construction obscures this deficiency by stating that "data lines" are "***lines*** to which the data driver supplies gradation sequence signals and applies a precharge voltage." This use of the plural studiously, and inappropriately, leaves out the requirement that *each* data line carries both types of signals. If Solas intends that some "data lines" can carry only precharge voltages and other "data lines" can carry only gradation sequence signals, such an interpretation would be flatly inconsistent with the intrinsic evidence and incorrect.

Solas's brief only disputes the requirement that each data line "connect[] a data driver to plurality of light emission drive circuits." Op. Br., 27. Yet Solas's expert admits that each data line is connected to a plurality of pixels, Ex. 3, 71:9–13, and, further, every embodiment discloses that each data line is connected to a plurality of light emission drive circuits (*i.e.,* pixel circuits). *See, e.g.*, Ex. 2, 34:52–35:10; Figs. 15–16. Nonetheless, whether the data line must be connected to a plurality of light emission drive circuits or can be connected to a single light emission drive circuit is not central to the dispute over this term. Defendants would thus be amenable to revising their construction to "conductive lines each of which connects a data driver to <u>one or more</u> light emission drive circuits and carries both a gradation sequence signal and precharge voltage" if it would avoid dispute over this term.

III. CONCLUSION

For these reasons, Defendants respectfully request that the Court adopt their constructions.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of the foregoing document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this February 16, 2022.

/s/ Melissa R. Smith
Melissa R. Smith